IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A radio transmitter, comprising:

a digital processor that receives digital data, that digitally modulates the digital data to produce a digital information signal, and that compensates the digital information signal to produce a pre-compensated digital information signal that is pre-compensated for group delay variation and magnitude response characteristics of at least one downstream filter;

a digital-to-analog converter (DAC) that receives the pre-compensated digital information signal and that converts the pre-compensated digital information signal to produce a continuous waveform analog signal;

a downstream filter that filters the continuous waveform analog signal to produce a filtered continuous waveform analog signal; and

phase locked loop circuitry (PLL) that receives the filtered continuous waveform analog signal to produce an output information signal in a selected frequency band.

2. (Original) The radio transmitter of claim 1 wherein the continuous waveform signal is produced to the PLL as the reference signal.

3. (Original) The radio transmitter of claim 1 wherein the pre-compensated digital information signal is a digital IF signal having a bandwidth in the range of 200 kHz to 300 kHz.

4. (Original) The radio transmitter of claim 1 wherein the pre-compensated digital information signal is a digital baseband signal.

5. (Original) The radio transmitter of claim 1 wherein the digital modulation scheme is constant envelope.

6. (Original) The radio transmitter of claim 1 wherein the pre-compensated digital information signal is an intermediate frequency baseband signal.

7. (Original) The radio transmitter of claim 1 wherein the PLL comprises:

a phase-frequency detector (PFD) coupled to receive the continuous waveform signal and coupled to receive a feedback signal, the PFD producing an error signal based at least in part on one of a phase or frequency of the feedback signal;

a charge pump for producing an error current responsive to the error signal;

a narrow band loop filter for converting the error current to an error voltage signal over a narrow frequency bandwidth;

an oscillator for producing an oscillation corresponding to a magnitude of the error voltage signal; and

mixer and filter circuitry for down converting and filtering the oscillation to produce the feedback signal.

8. (Original) The radio transmitter of claim 1 wherein the digital processor adds frequency selective magnitude pre-compensation and frequency selective group delay pre-compensation to selective frequency components of the digital data to reduce magnitude distortion and group delay variation produced within the PLL.

9. (Original) The radio transmitter of claim 1 wherein the digital processor includes a fourth order non-linear IIR filter that reduces group delay variation based on frequency..

10. (Original) The radio transmitter of claim 1 wherein digital processor further produces digital data having a magnitude response that is substantially inverted to a magnitude response of the PLL for a specified frequency band of interest wherein the PLL is coupled downstream of the digital processor and wherein the digital processor compensates for narrow band distortion produced by the downstream PLL.

11. (Original) A method for producing a continuous wave intermediate frequency (IF) signal, comprising:

filtering and partially distorting, in a narrow band loop filter of a PLL, a continuous waveform signal;

filtering frequency components produced by a PLL reference signal, in the narrow band loop filter of the PLL, spurious harmonic tones of a specified signal of interest;

producing, in a digital processor, a magnitude response that is substantially inverted to a magnitude response of the PLL for a specified frequency band of interest to compensate for the partial distortion by the loop filter of the PLL of the continuous waveform signal.

12. (Original) The method of claim 11 further comprising reducing group delay variation by producing, in the digital processor, delay for specified frequency components of the digital data.

13. (Original) The method of claim 12 further comprising adding frequency selective phase pre-compensation to compensate for group delay variation and magnitude distortion by the PLL to produce an output signal with reduced distortion.

14. (Original) A radio transmitter, comprising:

a digital-to-analog converter (DAC) coupled to receive a pre-compensated digital information signal, the DAC for producing a continuous waveform signal based on the pre-compensated digital information signal;

a low pass filter for producing a filtered continuous waveform signal based upon the continuous waveform signal produced by the DAC;

phase locked loop circuitry further including:

a phase-frequency detector (PFD) coupled to receive the continuous waveform signal and a feedback signal, the PFD producing an error signal based at least in part on a phase or frequency of the feedback signal;

a charge pump for producing an error current based on the error signal;

a narrow band loop filter for converting the error current to an error voltage signal;

an oscillator for producing an oscillation based upon a magnitude of the error voltage signal; and

mixer and filter circuitry for down converting and filtering the oscillation to produce the feedback signal; and

a digital processor for producing the pre-compensated digital information signal, the digital processor further comprising:

PLL magnitude equalizer for producing a magnitude response that is substantially inverted to a PLL magnitude response for a specified frequency band; and

a TX chain group delay equalizer for reducing overall group delay variation.

15. (Currently amended) The radio transmitter of claim ~~13~~14 wherein the TX chain group delay equalizer in the digital processor produces delay for specified frequency components of the pre-compensated digital information signal.

16. (Original) The radio transmitter of claim 14 wherein the TX chain group delay equalizer and the PLL magnitude equalizer are a fourth order IIR filters.

17. (Original) The radio transmitter of claim 14 wherein the digital processor further includes:

a baseband band data generator for producing digital data;

a first digital filter for interpolating the digital data to increase a sample rate of the digital data by a first factor value, the digital filter producing first upsampled digital data; and

a Gaussian filter for producing Gaussian filtered digital data from the upsampled digital data.

18. (Original) The radio transmitter of claim 14 wherein the digital processor further includes an integration module for integrating the Gaussian filtered digital data.

19. (Currently amended) The radio transmitter of claim ~~15~~17 wherein the digital processor further includes:

a coordination rotation digital computer (CORDIC) module for generating I and Q vector rotated data components from the Gaussian filtered digital data;

a second digital filter for interpolating the I and Q vector rotated data components to increase a sample rate of the I and Q vector rotated data components by a second factor value, the digital filter producing upsampled I and Q data components;

second and third digital filters for interpolating the upsampled I and Q data components to increase a sample rate of the upsampled I and Q data components a second factor value, the digital filter producing upsampled I and Q data components;

a multiplication module for multiplying the upsampled I and Q data components with modulation data to produce quadrature I and Q data; and

a summing node for combining the quadrature I and Q data to produce the pre-compensated digital information signal.

20. (Original) The digital processor of claim 18 wherein the baseband digital data is produced at an approximate sample rate of 270.833 kHz and wherein a product of the first and second factor value result in the pre-compensated digital information signal having sample rates equal to one of 13 MHz, 26 MHz, 104 MHz or 338 MHz.